AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 0016 with the following paragraph:

[0016] The input/output data pins (DQ0 – DQ15) 130 – 132 of the memory device 100 are brought out for use in testing and generally accessing the device 100. The DQ pins 130 – 132 are each coupled to a data latch 135 – 137 that latch in data with clocking circuitry 160 ~~138~~. The input data is written to the memory device 100 with bit line drivers 138 – 140. Each data input is coupled to a separate bit line driver 138 – 140. The circuitry of a bit line driver is well known in the art and is not discussed further.